REMARKS

Reconsideration and re-examination are hereby requested.

Claims 1-14 stand rejected as being anticipated by Martin et al., (U.S. Patent No. 5,214,768).

Referring to FIGS. 5 and 6 of the patent application it is noted that there is a plurality of director boards $190_1 - 218_8$. It is noted that each board has a plurality of directors and a crossbar switch 320. The switch 320 has a pair of output/input ports 325_1, 325_2. The ports are coupled to the message network 160.

Referring now to the claims, claim 1 points out that the system interface includes:

> (a) a plurality of first director ***boards***, each ***one*** of the first director ***boards*** having:
>
> (i) a ***plurality of first directors***; ***and***
>
> (ii) a ***crossbar switch*** having input/output ports coupled to the first directors on such one of the first director boards and a pair of output/input ports;
>
> (b) a plurality of second director ***boards***, each ***one*** of the second directors boards having:
>
> (i) a ***plurality of second directors***; and
>
> (ii) a ***crossbar switch*** having input/output ports coupled to the second directors on such one of the second director boards and a pair of output/input ports; (emphasis added)

The Examiner states that the plurality of first director boards is element 12. However, element 12 is a host computer. Further, the Examiner than states that the plurality of first directors is elements 14, 16, 18 and 19; however, these are not on the boards 14. Applicant fails to find a plurality of director boards each with BOARD having a plurality of directors coupled to a crossbar switch on the board.

Reconsideration is hereby requested.

Claim 8 has similar limitations. Therefore, it is respectfully submitted that the claims 1-14 are not anticipated by Martin.

New claims 15- 28 have been added. Reference is made to FIG. 2. It is noted that e\ach director board has, in addition to having a plurality of directors and crossbar switch 320, a second switch 318. Referring to FIG.. 7, an exemplary one of the director boards, here board 190_1, is shown. It is noted that switch 318 is coupled to the memory 220.

Claims 15 and 22 point out that wherein the data transfer section is also coupled to the output/input port of the crossbar switch of each one of the plurality of first director boards and to the output/input port of the crossbar switch of each one of the plurality of second director boards.

It is respectfully submitted that such an arrangement is not described in Martin.

In the event any additional fee is required, please charge such amount to Patent and Trademark Office Deposit Account No. 50-0845.

Respectfully submitted,

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Attachment: Claim Mark Up Sheets
EMC2-044PUS-response to oa 10_22_02.doc

COMPARISON CLAIMS

1. (Amended) A system interface comprising:

(a) a plurality of first director boards, each one of the first director boards having:

(i) a plurality of first directors; and

(ii) a crossbar switch having input/output ports coupled to the first directors on such one of the first director boards and a pair of output/input ports;

(b) a plurality of second director boards, each one of the second directors boards having:

(i) a plurality of second directors; and

(ii) a crossbar switch having input/output ports coupled to the second directors on such one of the second director boards and a pair of output/input ports;

(c) a data transfer section having a cache memory, such cache memory being coupled to the plurality of first and second directors;

(d) a message network, operative independently of the data transfer section, coupled to the pair of output/input ports of each one of the directors boards of the plurality of first director boards and to the pair of output/input ports of each one of the directors boards of the plurality of second director boards; and

(e) wherein the first and second directors control data transfer between the first directors and the second directors in response to messages passing between the first directors and the second directors through the message network to facilitate data transfer between first directors and the second directors with such data passing through the cache memory in the data transfer section.

2. The system interface recited in claim 1 wherein each one of the first directors includes:

a data pipe coupled between an input of such one of the first directors and the cache memory;

a controller for transferring the messages between the message network and such one of the first directors.

3. The system interface recited in claim 1 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a controller for transferring the messages between the message network and such one of the second directors.

4. The system interface recited in claim 2 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a controller for transferring the messages between the message network and such one of the second directors.

5. The system interface recited in claim 1 wherein each one of the first directors includes:

a data pipe coupled between an input of such one of the first directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the first directors and for controlling the data between the input of such one of the first directors and the cache memory.

6. The system interface recited in claim 1 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the second directors

and for controlling the data between the input of such one of the second directors and the cache memory.

7. The system interface recited in claim 5 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the second directors and for controlling the data between the input of such one of the second directors and the cache memory.

8. (Amended) A data storage system for transferring data between a host computer/server and a bank of disk drives through a system interface, such system interface comprising:

(a) a plurality of first director boards coupled to host computer/server; each one of the first director boards having:

(i) a plurality of first directors; and

(ii) a crossbar switch having input/output ports coupled to the first directors on such one of the first director boards and a pair of output/input ports;

(b) a plurality of second director boards coupled to the bank of disk drives, each one of the second director boards having:

(i) a plurality of second directors; and

(ii) a crossbar switch having input/output ports coupled to the second directors on such one of the second director boards and a pair of output/input ports;

(c) a data transfer section having a cache memory, such cache memory being coupled to the plurality of first and second directors;

(d) a message network, operative independently of the data transfer section, coupled to the pair of output/input ports of each one of the directors boards of the plurality of

first director boards and to the pair of output/input ports of each one of the directors boards of the plurality of second director boards; and

(e) wherein the first and second directors control data transfer between the host computer and the bank of disk drives in response to messages passing between the first directors and the second directors through the message network to facilitate the data transfer between host computer/server and the bank of disk drives with such data passing through the cache memory in the data transfer section.

9. The system interface recited in claim 8 wherein each one of the first directors includes:

a data pipe coupled between an input of such one of the first directors and the cache memory;

a controller for transferring the messages between the message network and such one of the first directors.

10. The system interface recited in claim 8 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a controller for transferring the messages between the message network and such one of the second directors.

11. The system interface recited in claim 9 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a controller for transferring the messages between the message network and such one of the second directors.

12. The system interface recited in claim 8 wherein each one of the first directors includes:

a data pipe coupled between an input of such one of the first directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the first directors and for controlling the data between the input of such one of the first directors and the cache memory.

13. The system interface recited in claim 8 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the second directors and for controlling the data between the input of such one of the second directors and the cache memory.

14. The system interface recited in claim 12 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the second directors and for controlling the data between the input of such one of the second directors and the cache memory.

15. A system interface comprising:

(a) a plurality of first director boards, each one of the first director boards having:

(i) a plurality of first directors; and

(ii) a crossbar switch having input/output ports coupled to the first directors on such one of the first director boards and an output/input port;

(b) a plurality of second director boards, each one of the second directors boards having:

(i) a plurality of second directors; and

(ii) a crossbar switch having input/output ports coupled to the second directors on such one of the second director boards and an output/input port;

(f) a data transfer section having a cache memory, such cache memory being coupled to the plurality of first and second directors;

(g) wherein the data transfer section is also coupled to the output/input port of the crossbar switch of each one of the plurality of first director boards and to the output/input port of the crossbar switch of each one of the plurality of second director boards;

(h) a message network, operative independently of the data transfer section; and

(e) wherein the first and second directors control data transfer between the first directors and the second directors in response to messages passing between the first directors and the second directors through the message network to facilitate data transfer between first directors and the second directors with such data passing through the cache memory in the data transfer section.

16. The system interface recited in claim 15 wherein each one of the first directors includes:

a data pipe coupled between an input of such one of the first directors and the cache memory;

a controller for transferring the messages between the message network and such one of the first directors.

17. The system interface recited in claim 15 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a controller for transferring the messages between the message network and such one of the second directors.

18.. The system interface recited in claim 16 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a controller for transferring the messages between the message network and such one of the second directors.

19. The system interface recited in claim 15 wherein each one of the first directors includes:

a data pipe coupled between an input of such one of the first directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the first directors and for controlling the data between the input of such one of the first directors and the cache memory.

20. The system interface recited in claim 15 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the second directors and for controlling the data between the input of such one of the second directors and the cache memory.

21. The system interface recited in claim 19 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the second directors and for controlling the data between the input of such one of the second directors and the cache memory.

22. A data storage system for transferring data between a host computer/server and a bank of disk drives through a system interface, such system interface comprising:

(a) a plurality of first director boards coupled to host computer/server; each one of the first director boards having:

(i) a plurality of first directors; and

(ii) a crossbar switch having input/output ports coupled to the first directors on such one of the first director boards and an output/input port;

(b) a plurality of second director boards coupled to the bank of disk drives, each one of the second director boards having:

(i) a plurality of second directors; and

(ii) a crossbar switch having input/output ports coupled to the second directors on such one of the second director boards and an output/input port;

(d) a data transfer section having a cache memory, such cache memory being coupled to the plurality of first and second directors;

(d) wherein the data transfer section is also coupled to the output/input port of the crossbar switch of each one of the plurality of first director boards and to the output/input port of the crossbar switch of each one of the plurality of second director boards;

(e) a message network, operative independently of the data transfer section; and

(f) wherein the first and second directors control data transfer between the host computer and the bank of disk drives in response to messages passing between the first directors and the second directors through the message network to facilitate the data transfer between host computer/server and the bank of disk drives with such data passing through the cache memory in the data transfer section.

23. The system interface recited in claim 22 wherein each one of the first directors includes:

a data pipe coupled between an input of such one of the first directors and the cache memory;

a controller for transferring the messages between the message network and such one of the first directors.

24. The system interface recited in claim 22 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a controller for transferring the messages between the message network and such one of the second directors.

25. The system interface recited in claim 23 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a controller for transferring the messages between the message network and such one of the second directors.

26. The system interface recited in claim 22 wherein each one of the first directors includes:

a data pipe coupled between an input of such one of the first directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the first directors and for controlling the data between the input of such one of the first directors and the cache memory.

27. The system interface recited in claim 22 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the second directors and for controlling the data between the input of such one of the second directors and the cache memory.

28. The system interface recited in claim 26 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the second directors and for controlling the data between the input of such one of the second directors and the cache memory.